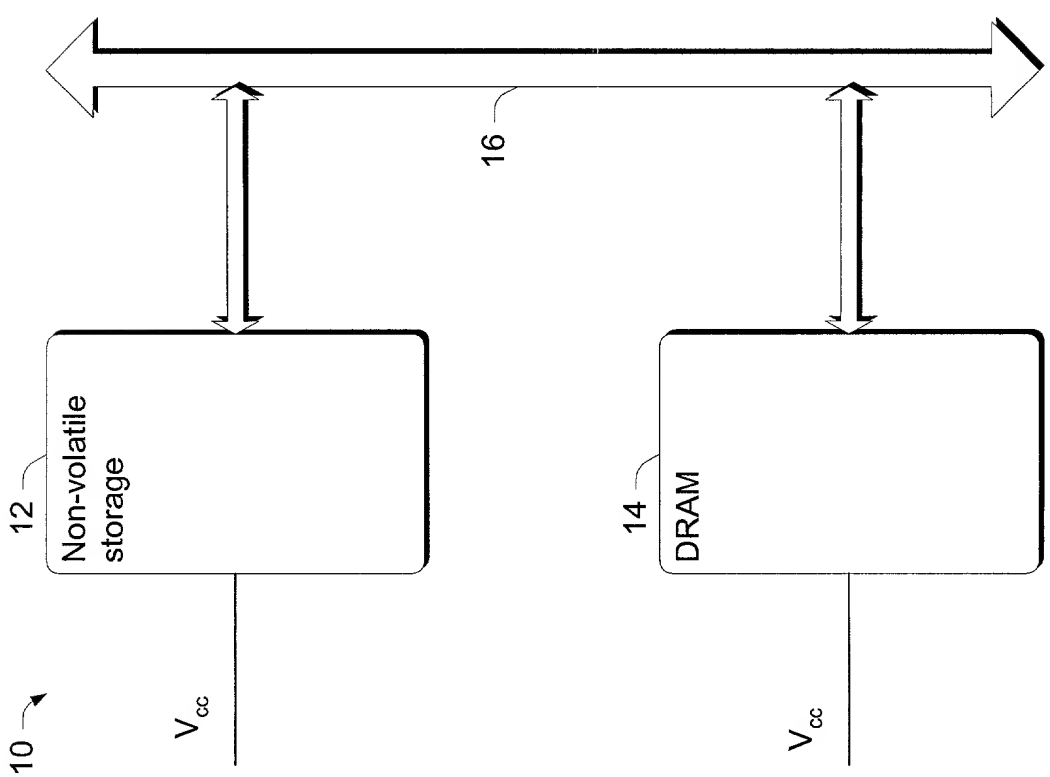

Fig. 1

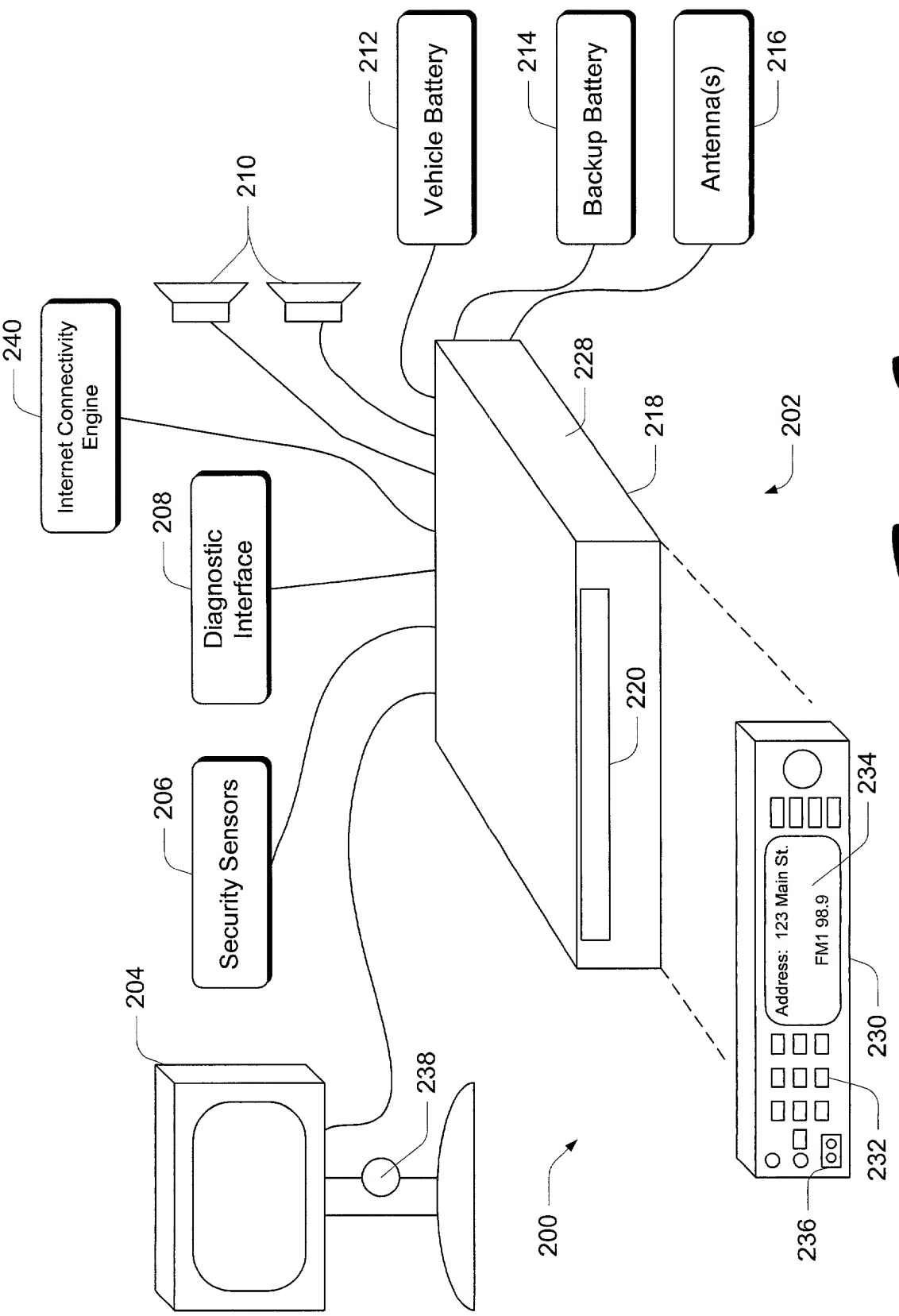
Internet Connectivity Engine
240
Diagnostic Interface
208
Security Sensors
206
210
Vehicle Battery
212
Backup Battery
214
Antenna(s)
216
228
218
202
220
204
238
200
Address: 123 Main St.
FM1 98.9
234
230
232
236

Fig. 2

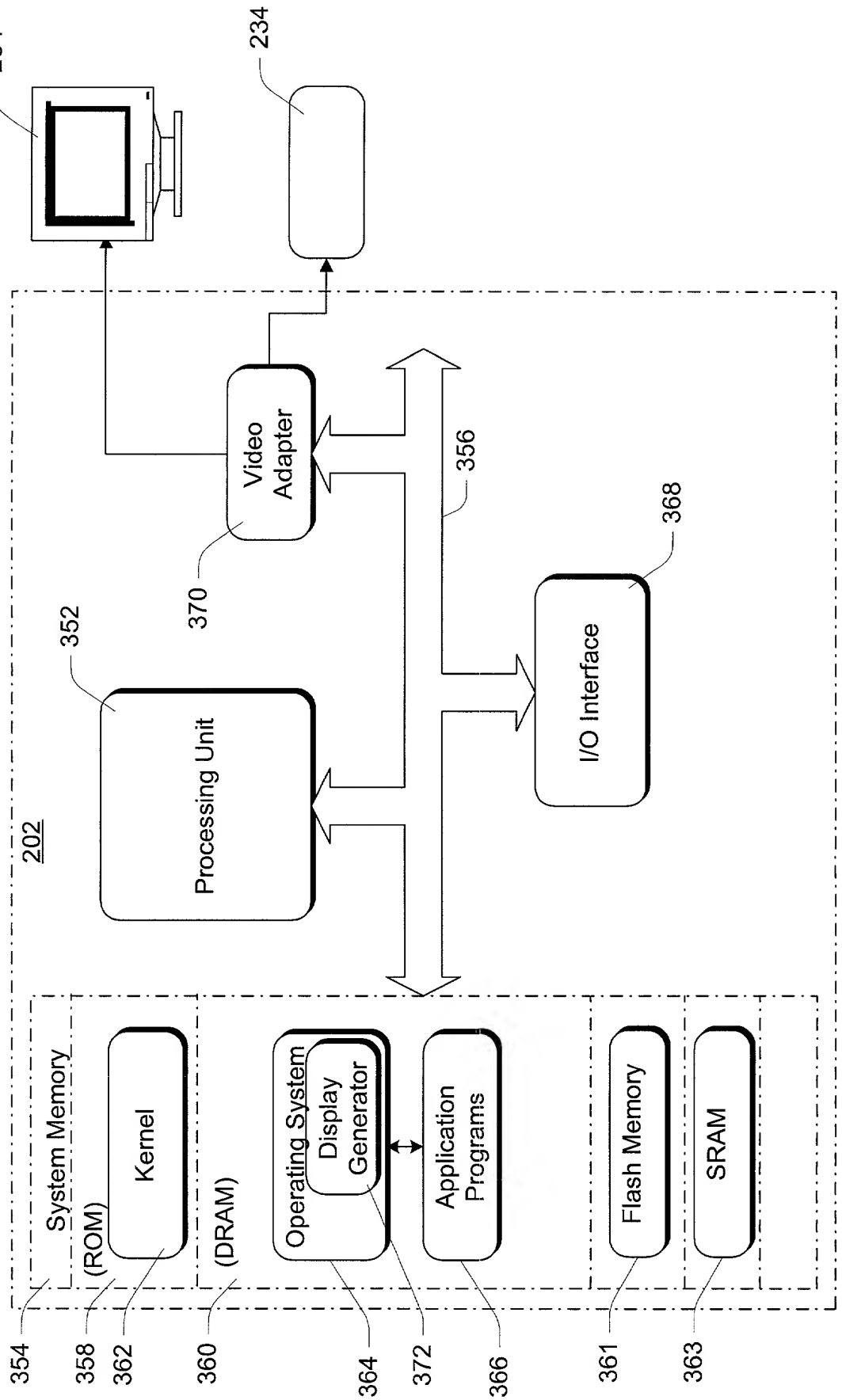
204
234
202
352
Processing Unit
370
Video Adapter
356
368
I/O Interface
System Memory
(ROM)
Kernel
(DRAM)
Operating System
Display Generator
Application Programs
Flash Memory
SRAM
354
358
362
360
364
372
366
361
363

Fig. 3

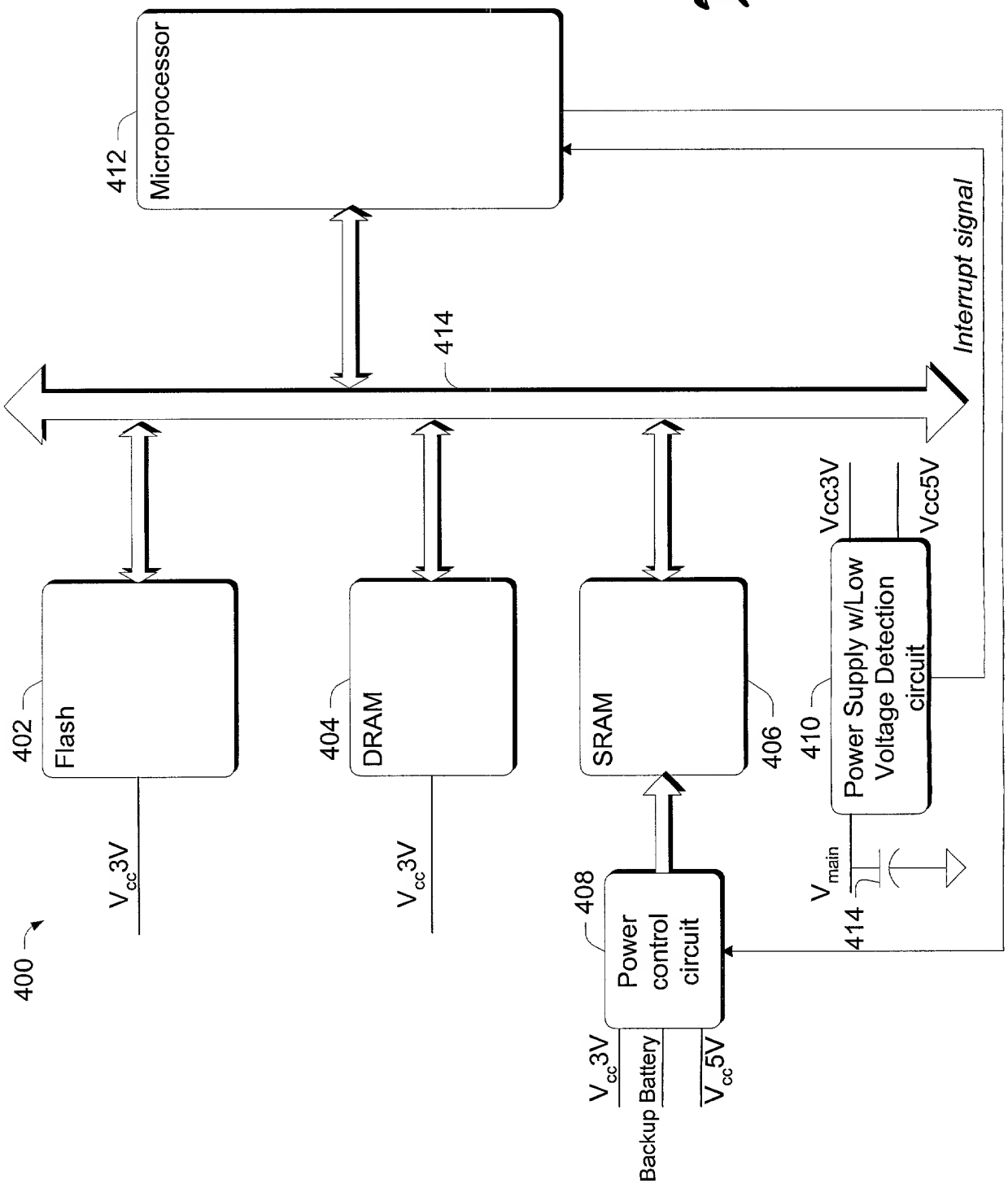
400
412
Microprocessor
414
Interrupt signal
402
Flash
V_{cc}3V
404
DRAM
V_{cc}3V
SRAM
406
410
Power Supply w/Low Voltage Detection circuit
Vcc3V
Vcc5V
V_{main}
414
408
Power control circuit
V_{cc}3V
Backup Battery
V_{cc}5V

Fig. 4

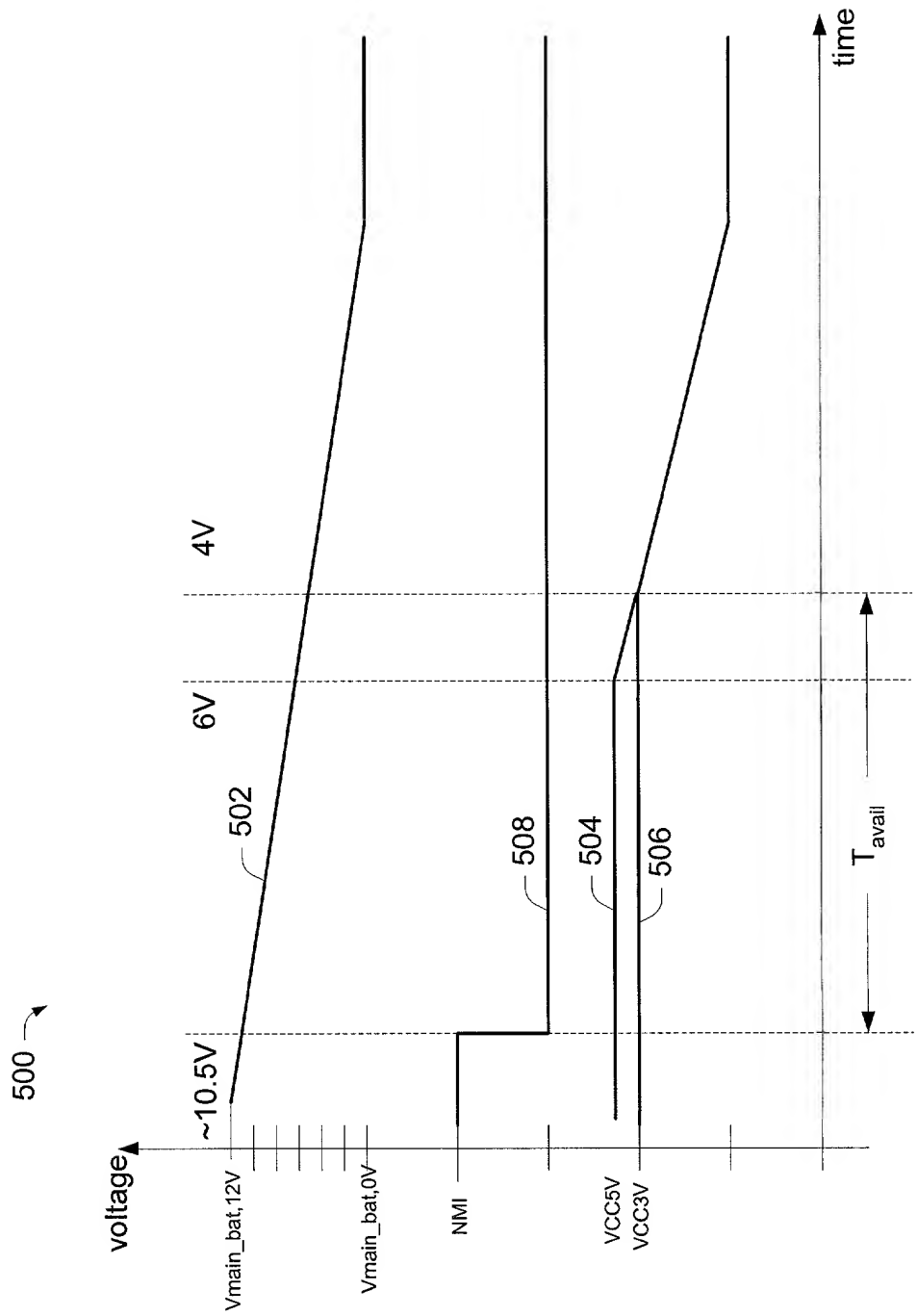
500
voltage
time
~10.5V
6V
4V
502
508
504
506
Vmain_bat,12V
Vmain_bat,0V
NMI
VCC5V
VCC3V
T_{avail}

Fig. 5

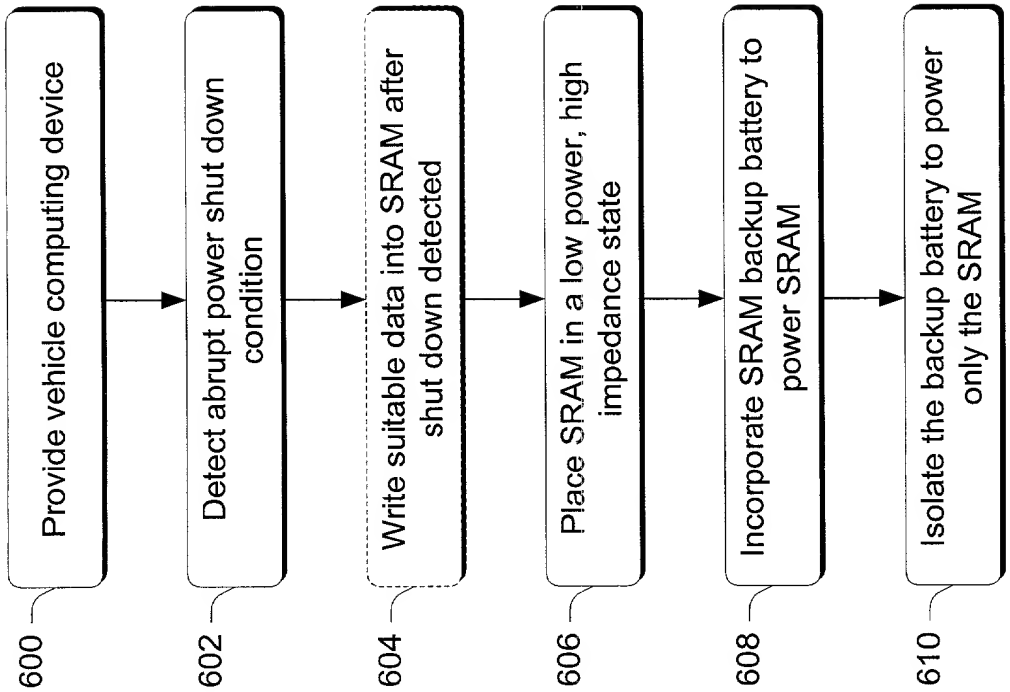
Provide vehicle computing device
Detect abrupt power shut down condition
Write suitable data into SRAM after shut down detected
Place SRAM in a low power, high impedance state
Incorporate SRAM backup battery to power SRAM
Isolate the backup battery to power only the SRAM
600
602
604
606
608
610

Fig. 6

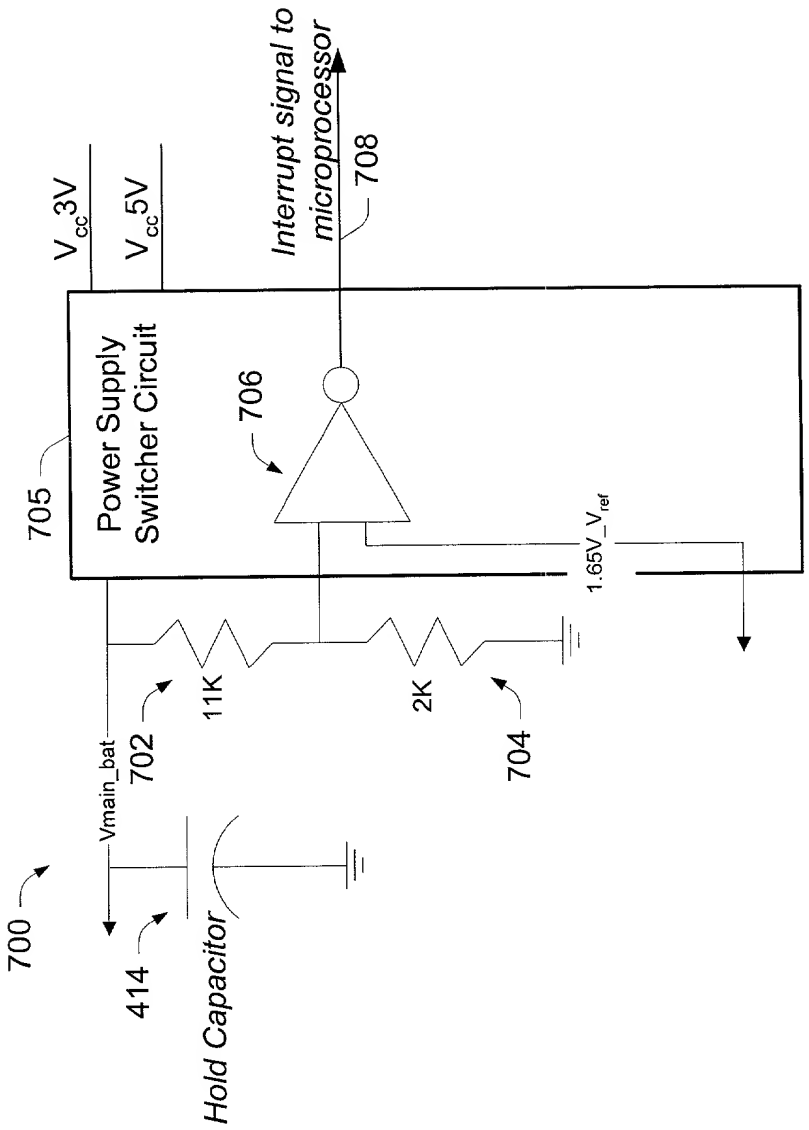
700
414
Hold Capacitor
Vmain_bat
702
11K
2K
704
705
Power Supply
Switcher Circuit
706
1.65V_Vref
Vcc3V
Vcc5V
Interrupt signal to
microprocessor
708

Fig. 7

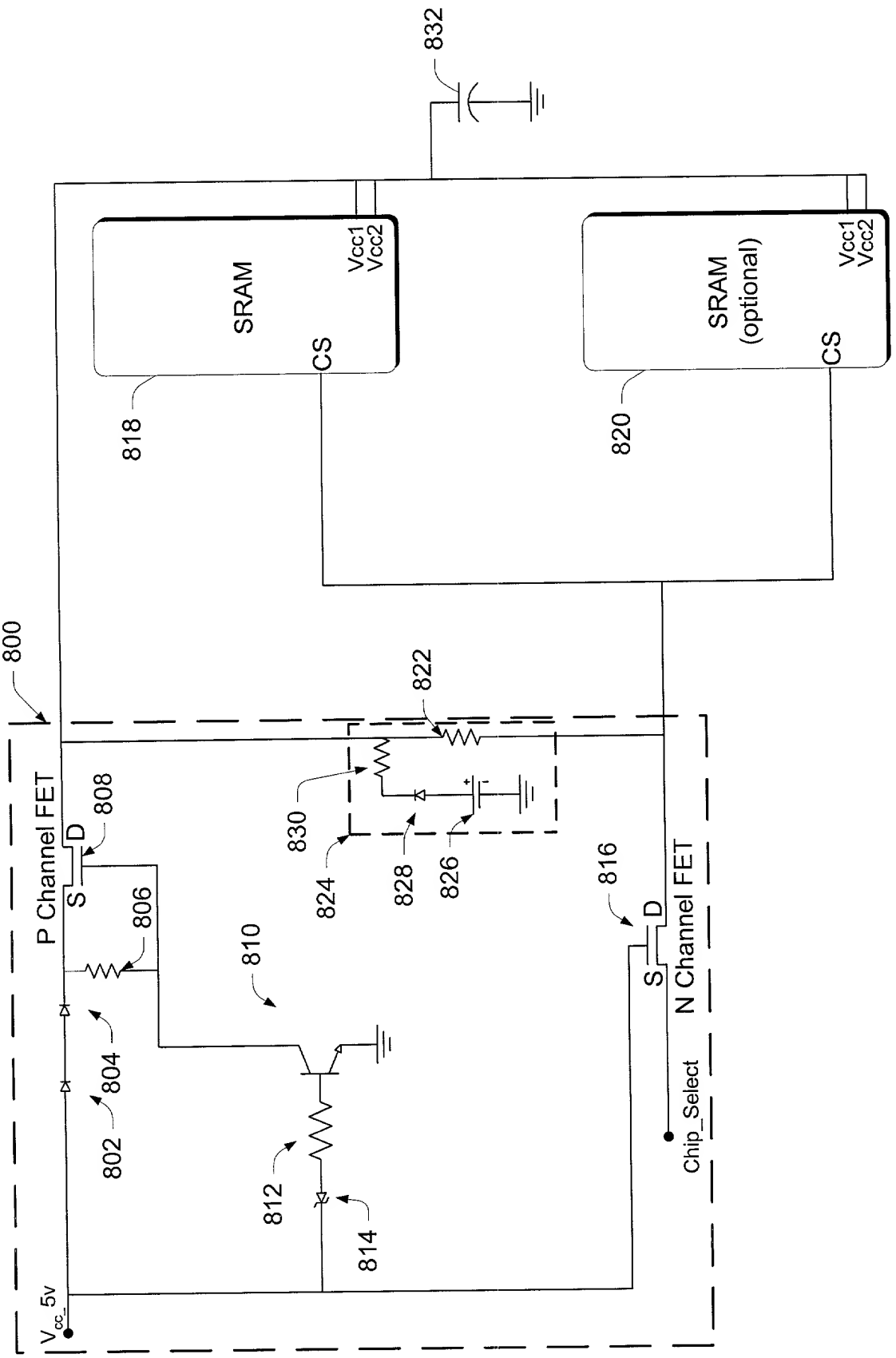
832
SRAM
Vcc1
Vcc2
CS
818
SRAM
(optional)
Vcc1
Vcc2
CS
820
800
822
830
824
828
826
P Channel FET
808
D
S
806
810
804
802
812
814
816
D
S
N Channel FET
Chip_Select
Vcc_5v

Fig. 8

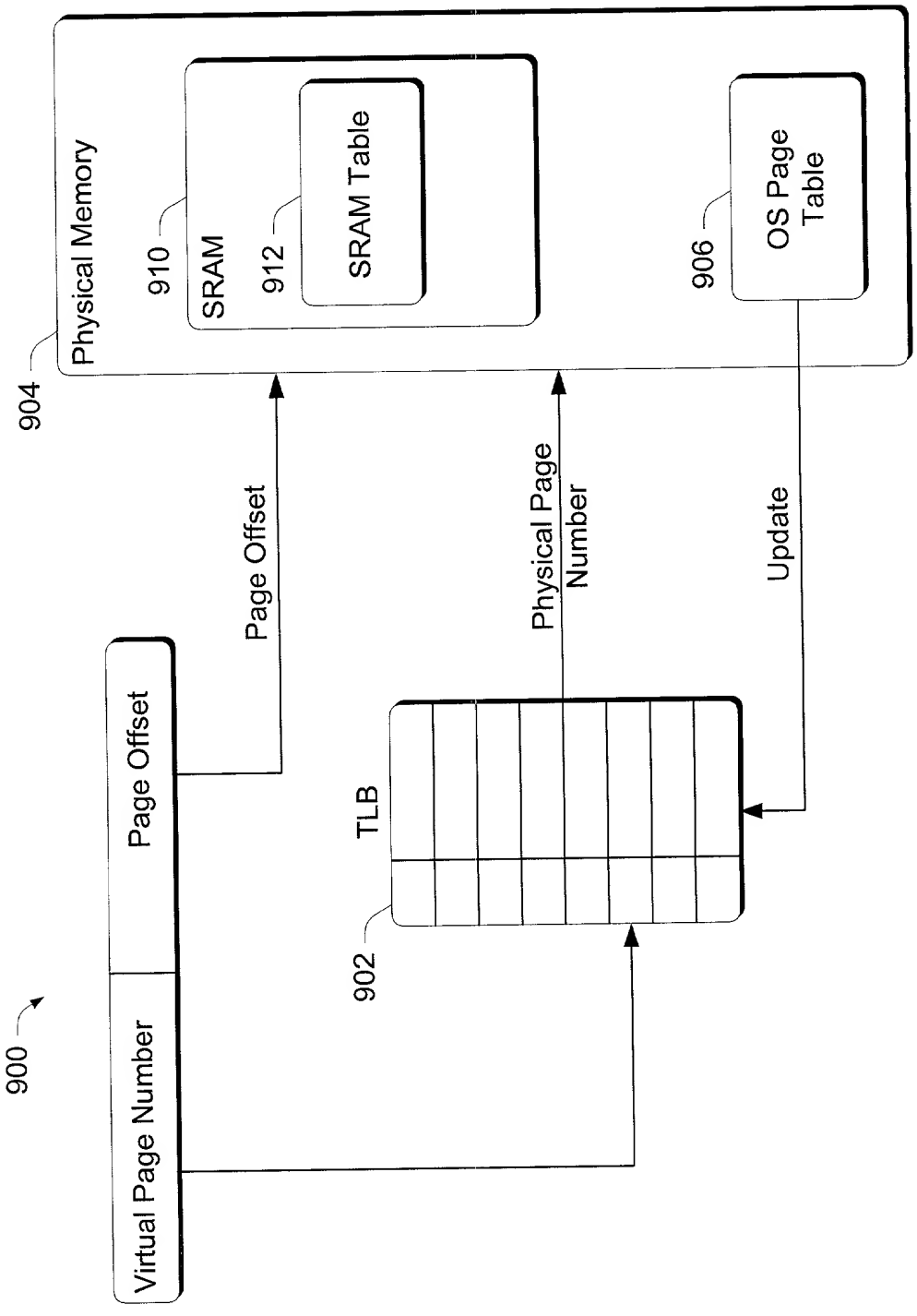
900
Virtual Page Number
Page Offset
Page Offset
TLB
902
Physical Page Number
Update
904
Physical Memory
910
SRAM
912
SRAM Table
906
OS Page Table

Fig. 9

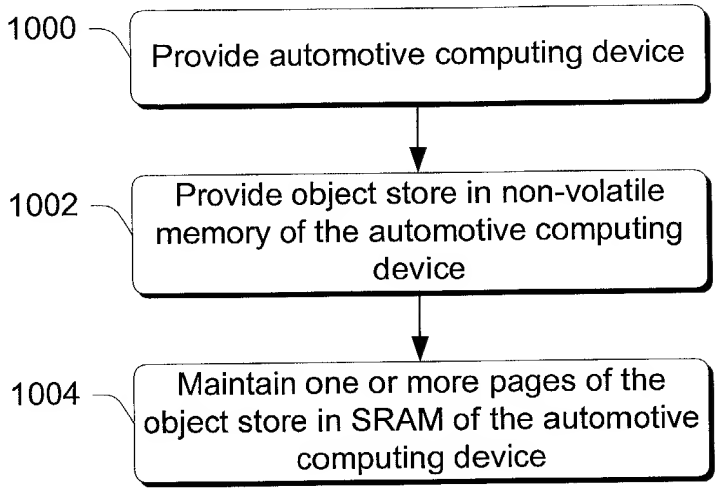
1000
Provide automotive computing device
1002
Provide object store in non-volatile memory of the automotive computing device
1004
Maintain one or more pages of the object store in SRAM of the automotive computing device

Fig. 10

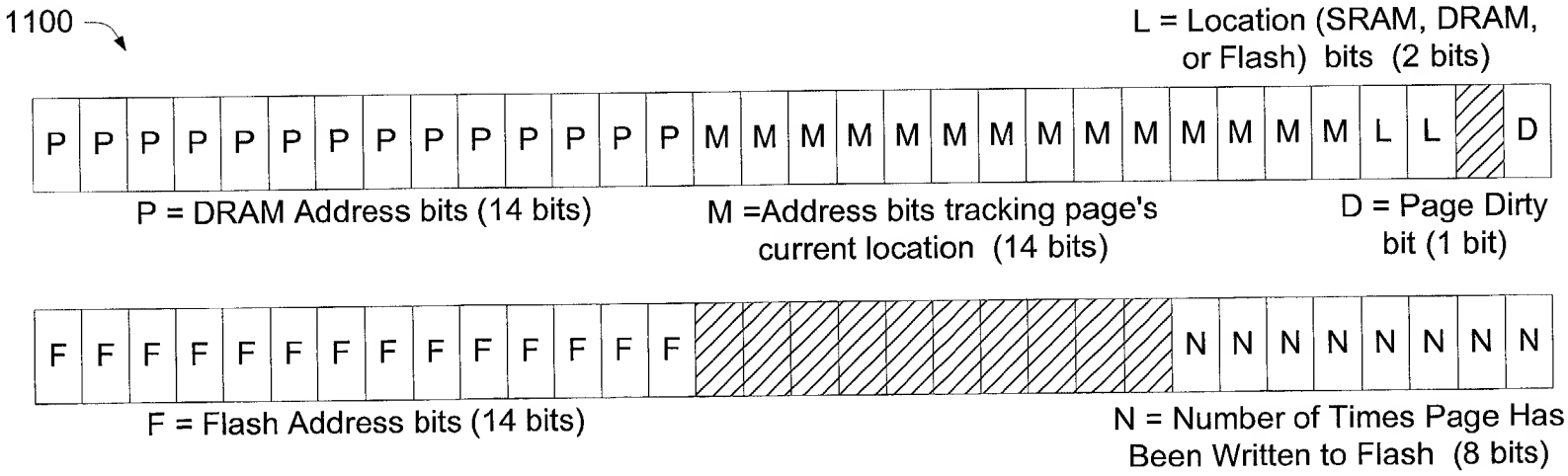
1100
L = Location (SRAM, DRAM, or Flash) bits (2 bits)
P P P P P P P P P P P P P P M M M M M M M M M M M M M M L L D
P = DRAM Address bits (14 bits)
M =Address bits tracking page's current location (14 bits)
D = Page Dirty bit (1 bit)
F F F F F F F F F F F F F F N N N N N N N N
F = Flash Address bits (14 bits)
N = Number of Times Page Has Been Written to Flash (8 bits)

Fig. 11

Handling Object Store Page Exception

Exception Type	Current Access for OS page	Current Location of OS page	Action	Additional Notes
Write	Write	SRAM	No special action is required. This is a normal TLB miss. OS page table information must be fetched and stored inside the TLB. No interaction with the SRAM object store page table is required	Since the TLB has a limited number of entries, repeated page table misses can happen often
Read	Read	DRAM or SRAM	No special action is required. This is a normal TLB miss. OS page table information must be fetched and stored inside the TLB. No interaction with the SRAM object store page table is required	Since the TLB has a limited number of entries, repeated page table misses can happen often
Read	Read	Flash	(1) Copy the page into DRAM at physical address specified in the OS page table. (The faulting virtual address is used as a key into the OS page table in which the corresponding physical address is stored). (2) Modify the OS page table and TLB permissions for read-only accesses. (3) Copy the M bits to the F bits in order to specify where the page is located in flash in case of power loss. Modify the L bits to indicate that the page is now in DRAM. (4) Modify the SRAM object store page table M bits to specify the physical address in DRAM.	The access bits are changed to read only so that an attempt to write to the page will cause a write exception. In this exception handler, the page can be copied to SRAM before writing to it (thus making it dirty).

Fig. 12

Exception Type	Current Access for OS page	Current Location of OS page	Action	Additional Notes
Write or Read/write	Read	Flash	(1) Copy the page into SRAM at an available page slot. (2) Update the OS page table and the TLB physical address values to the page's address in SRAM. (3) Modify the OS page table and the TLB permissions for the access desired. (4) Modify the SRAM object store page table M bits to specify the physical address in SRAM. Modify the L bits to indicate that the page is now in SRAM. (5) Modify the SRAM page table, TLB, and OS page table access bits for the desired access.	The access bits are changed to read only so that an attempt to write to the page will cause a write exception. In this exception handler, the page can be copied to SRAM before writing to it (thus making it dirty).
Write or Read/write	Read	DRAM	See directly above	See directly above

Fig. 12 (cont.)

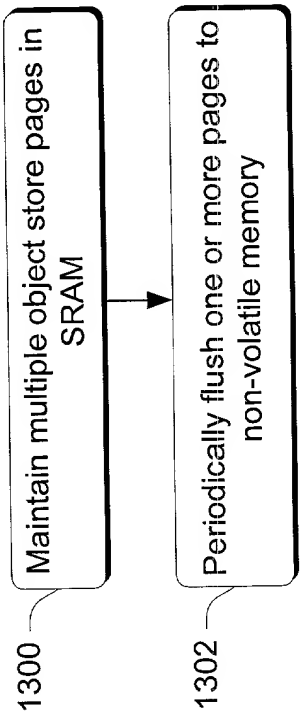
Maintain multiple object store pages in SRAM
Periodically flush one or more pages to non-volatile memory
1300
1302

Fig. 13

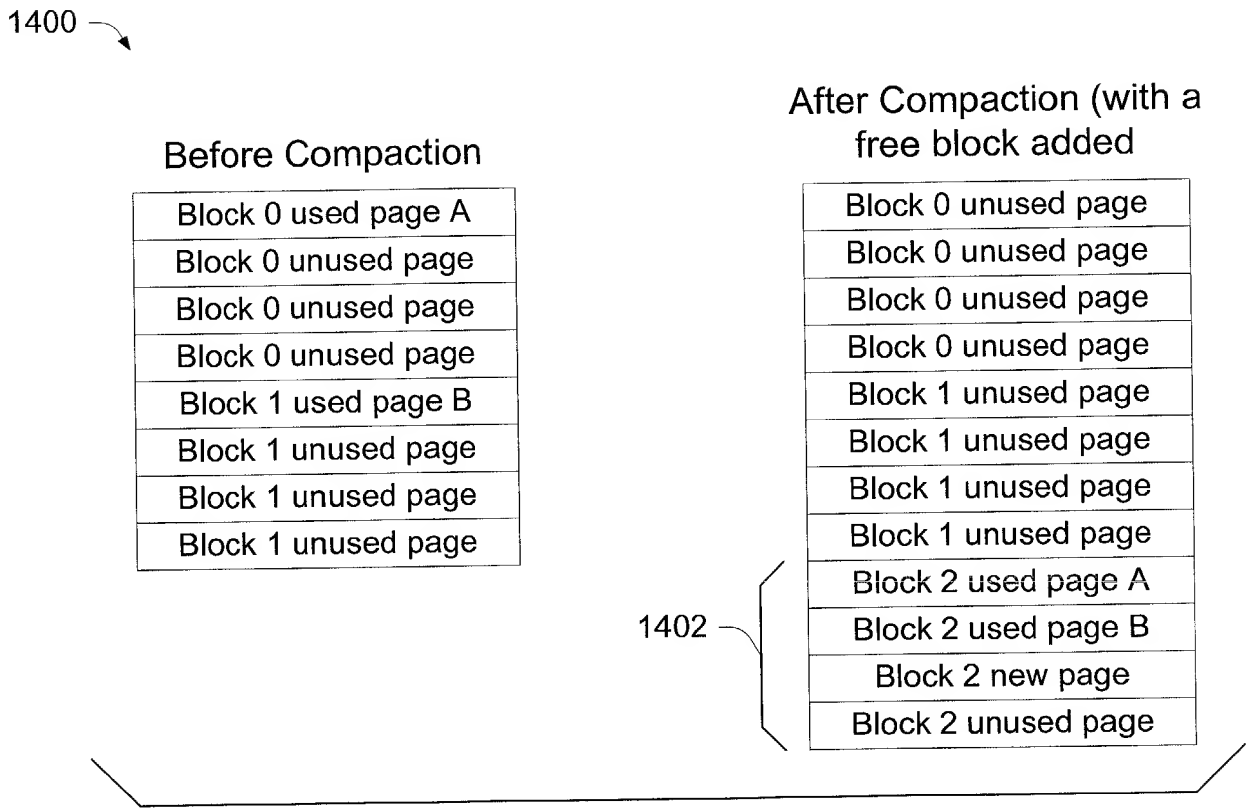
1400
Before Compaction
Block 0 used page A
Block 0 unused page
Block 0 unused page
Block 0 unused page
Block 1 used page B
Block 1 unused page
Block 1 unused page
Block 1 unused page
After Compaction (with a free block added
Block 0 unused page
Block 0 unused page
Block 0 unused page
Block 0 unused page
Block 1 unused page
Block 1 unused page
Block 1 unused page
Block 1 unused page
Block 2 used page A
Block 2 used page B
Block 2 new page
Block 2 unused page
1402

Fig. 14

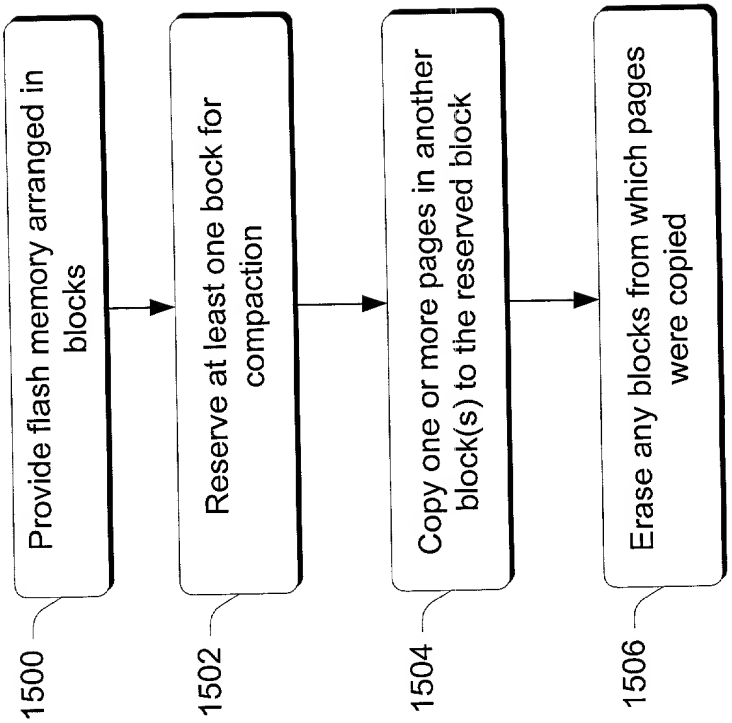
Provide flash memory arranged in blocks
Reserve at least one bock for compaction
Copy one or more pages in another block(s) to the reserved block
Erase any blocks from which pages were copied
1500
1502
1504
1506

Fig. 15

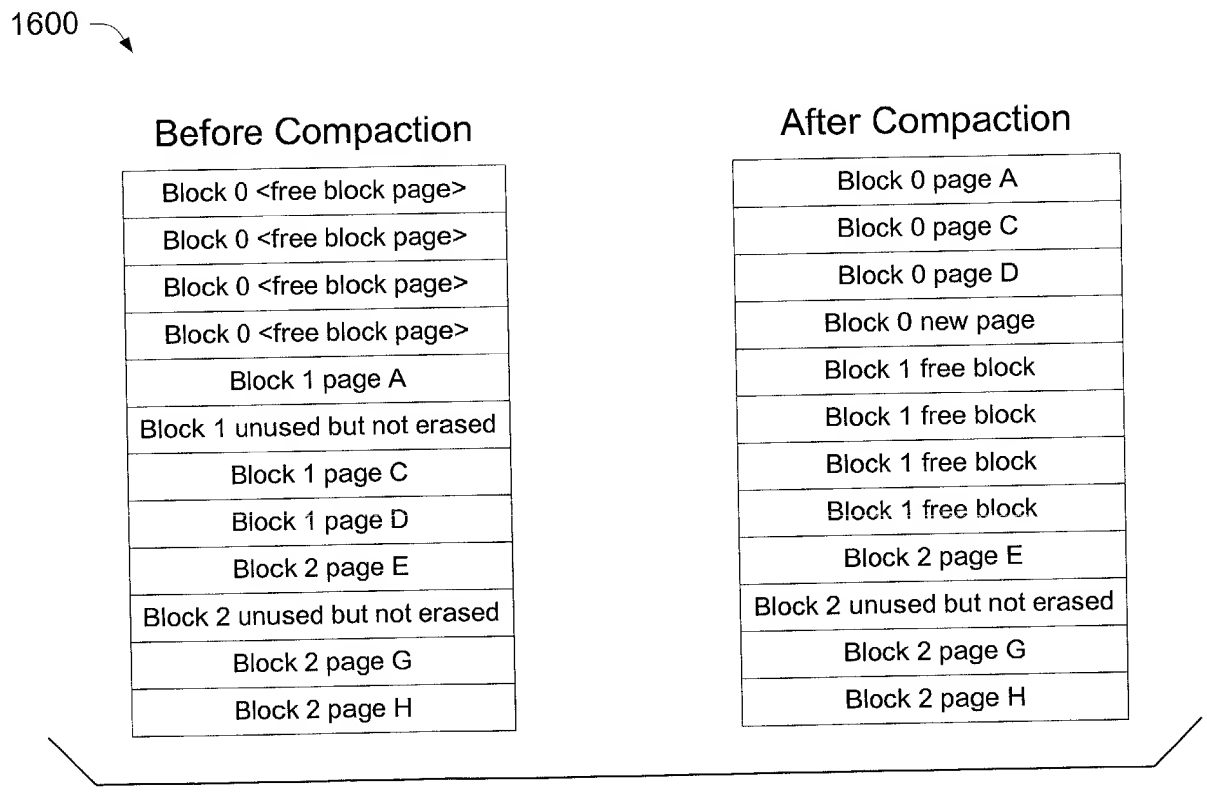
1600
Before Compaction
Block 0 <free block page>
Block 0 <free block page>
Block 0 <free block page>
Block 0 <free block page>
Block 1 page A
Block 1 unused but not erased
Block 1 page C
Block 1 page D
Block 2 page E
Block 2 unused but not erased
Block 2 page G
Block 2 page H
After Compaction
Block 0 page A
Block 0 page C
Block 0 page D
Block 0 new page
Block 1 free block
Block 1 free block
Block 1 free block
Block 1 free block
Block 2 page E
Block 2 unused but not erased
Block 2 page G
Block 2 page H

Fig. 16

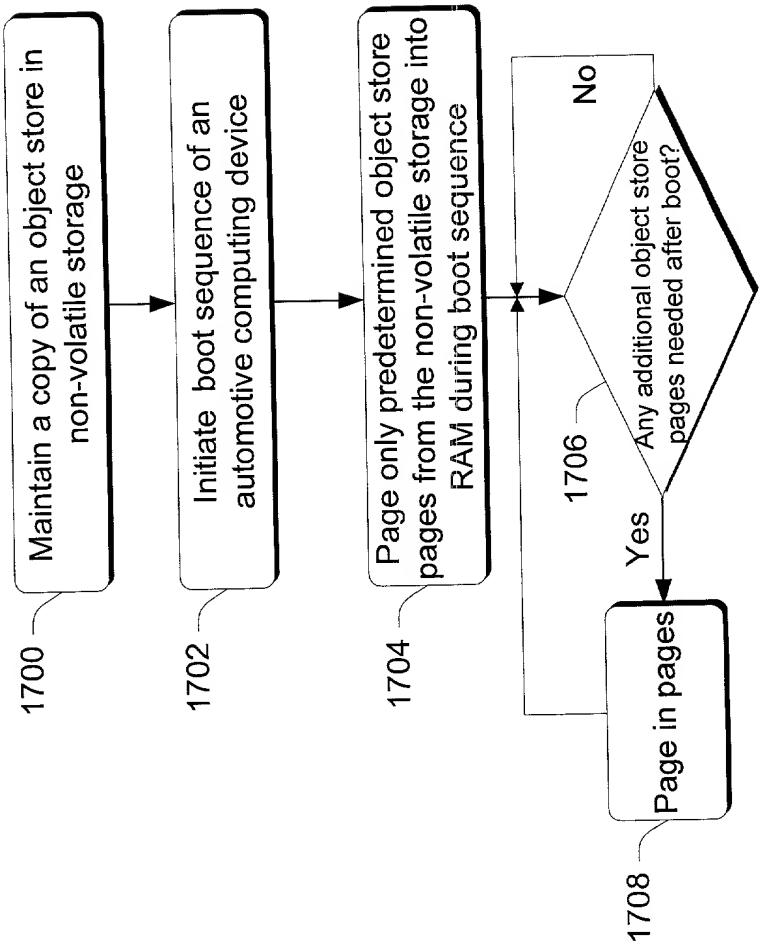
Maintain a copy of an object store in non-volatile storage
1700
Initiate boot sequence of an automotive computing device
1702
Page only predetermined object store pages from the non-volatile storage into RAM during boot sequence
1704
Any additional object store pages needed after boot?
1706
No
Yes
Page in pages
1708

Fig. 17